Abstract of the Disclosure

A memory system having at least one memory subsystem and using a packet protocol communicated over a command and address bus and at least one data bus. The memory subsystems are pipelined to achieve wide data paths and to support a high number of memory devices, such as dynamic random access memory devices, per data bus. The packet protocol is defined to compensate for the delay stages of the pipelined memory subsystem in order to optimize the access time of the memory devices.

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